இந்திய தகவல் தொழில்நுட்பக் கழகம், திருச்சிராப்பள்ளி
भारतीय सूचना प्रौद्योगिकी संस्थान, तिरुचिरापल्ली
INDIAN INSTITUTE OF INFORMATION TECHNOLOGY TIRUCHIRAPPALLI
(An Institute of National Importance under MoE, Govt. of India)
SETHURAPATTI, TRICHY-MADURAI HIGHWAY, TIRUCHIRAPPALLI 620012
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Advt. No. IIITT/SMDP/JRF/PA/2024/10-01 **Dated: 14.10.2024**

ROLLING ADVERTISEMENT FOR THE POST OF PROJECT ASSISTANT AND JRF UNDER C2S PROJECT

Applications are invited from Indian Citizens for the JRF & PA for project entitled "**Ultra Low Power SHAKTI RISC V Based Lightweight Edge AI Processor for IoT enabled Healthcare Applications**" under Chip-to-Startup (C2S) programme (Category –II) funded by the Ministry of Electronics & Information Technology (MeitY), Govt. of India. The details are as follows:

1.	**Name of the Position**	Project Assistant (PA) & Junior Research Fellowship (JRF)
2.	**Duration of the Project**	Initially for One Year. Extendable up to next four years based on the performance after a review. (Total Project duration is 5 years i.e., 2024 – 2029)
3.	**Essential Qualifications**	**i.** First class in B.E/B.Tech. - Electronics and Communication Engineering / Electrical and Electronics Engineering / Computer Science and Engineering with minimum of 60% of marks or 6.5 CGPA from any recognized university / Institute. **AND** **ii.** First class in M.E/M.Tech. - VLSI/ Microelectronics/ SoC-Design/ Embedded systems/ Semiconductor Technology/ IoT/ Computer Science and Engineering / Artificial Intelligence and Machine Learning/Signal Processing/ Communication systems with minimum of 60% of marks or 6.5 CGPA from any recognized university / Institute.
4.	**Emoluments**	Rs. 15,000 – 20,000/- per month (Project Assistant) Rs. 30,000 – 37,000/- per month (JRF)
5.	**Skill Set Required**	• Sound Knowledge of Verilog RTL Coding, Strong fundamentals in C/C++, MATLAB, AI algorithm implementation in C/Python, Multi-threading and Programming, Good knowledge in Linear algebra, Knowledge in Digital signal processing, adaptive signal processing & array signal processing. • Hands on experience in FPGA Architecture and Programming, Hands on experience on AI based Micro-controllers and Microprocessors Programming and debugging, Hands on experience in IoT based electronic product design and development, Sensors and actuators used in healthcare applications and interfacing with microprocessors and micro-controllers. • Profound knowledge on ASIC Design and Implementation (RTL coding to GDS II Extraction), Network/System on Chip • Basic Knowledge on EDA tools
6.	**Date & Time of Interview**	***Will be intimated later through email***

7.	**Venue**	***Room No: 418, Sir C.V. Raman Academic and Administrative Block, IIIT Tiruchirappalli, Sethurapatti, Tiruchirappalli - 620012***
8.	**Selection Process**	Written test followed by interview. **Note:** ***candidates with valid gate score are eligible to get the fellowship as per DST norms***
9.	**Last date for Applying**	Applications will be reviewed on a rolling basis. However, applications received on or before **16.12.2024** will be considered for the first level of interviews.

Note:

1. Eligible candidates are required to attend the interview **with all original academic and experience certificates** (if any) and a **valid photo identity proof**.
2. **Further, bring <u>one set of photo copy</u> of the testimonials mentioned below.**

Details of the Documents/Testimonials	Online Submission Procedure
a. Detailed CV/Resume* **b. SSLC Marksheet*** **c. HSLC Marksheet (or) Diploma Consolidated Marksheet & Degree*** **d. B.E/B.Tech Consolidated Marksheet & Degree*** **e. M.E/M.Tech Consolidated Marksheet & Degree* (not applicable for those applying for Project Assistant post)** **f. UG/PG Transfer Certificate*** **g. GATE/CSIR-UGC NET Score Card (if any)** **h. Work Experience Certificates (if any)** **i. Research Experience Certificates (if any)** **j. Community Certificate (if applicable)** **k. Valid Government ID proof***	**Kindly fill in the google forms link given below:** https://forms.gle/sWBxG81raNvaCQ9dA

***Mandatory**

3. Candidates before appearing for the selection process shall ensure that they are eligible for the position they intend to apply.
4. The post will be tenable initially for a period of one year. It may be extended further at the discretion of duly constituted committee of IIITT.
5. The fellowship can be terminated with a 30-day notice before the completion of the tenure if the performance till date is not satisfactory.
6. **Selected candidates with M.E/M.Tech Qualification may be allowed to join PhD program under project category as per the Institute's norms.**
7. The shortlisted candidates will be intimated about the selection process through e-mail.
8. No TA/DA is admissible for attending the selection process.
9. The decision of the selection committee is final.
10. Canvassing in any form leads to the rejection of the candidature.
11. The tenure of the project staff is co-terminus with the project.
12. IIIT Tiruchirappalli does not bear any implications/obligations on the recruited Project staff in a given project.
13. Selected candidates will not be permitted to claim any regular/part-time appointments in this institute or any other during this period.
14. The Institute reserves the right not to fill up the posts, cancel the advertisement in whole or in part, without assigning any reason and the decision of the Director of IIIT Tiruchirappalli, in this regard shall be final.

C2S Project Team